What is claimed is:

CLAIMS

1. A computer system comprising:

a system fabric;

a plurality of cell boards connected to the system fabric, each of the plurality of cell boards comprising:

at least one microprocessor;

a memory;

a microcontroller coupled between the memory and the at least one microprocessor;

a fabric agent chip coupled between the microcontroller and the system fabric; and

a compression/decompression (codec) engine coupled between the microcontroller and the fabric agent chip.

2. The computer system of claim 1, wherein the system fabric comprises a crossbar switch.

3. The computer system of claim 1, wherein the system fabric comprises a bus.

4. The computer system of claim 1, wherein each of the plurality of cell boards includes a plurality of processors.

5. The computer system of claim 1, wherein the codec engine in each of the plurality of cell boards comprises:

means for compressing data transmitted by the memory controller to the fabric agent chip; and

means for decompressing data transmitted by the fabric agent chip to the memory controller.

6. The computer system of claim 1 wherein the fabric agent chip includes the codec engine.

7. A computer system comprising:

a system fabric;

a plurality of cell boards, each of the plurality of cell boards comprising:

at least one processor;

a memory;

memory control means, coupled between the memory and the at least one microprocessor, for controlling communication between the at least one processor and the memory;

communication means, coupled between the microcontroller and the system fabric, for controlling communication between the microcontroller and the system fabric; and

compression/decompression means, coupled between the memory control means and the communication means, for compressing communications received by the communication means over the system fabric and for decompressing communications transmitted by the communication means over the system fabric.

8. The computer system of claim 7, wherein each of the plurality of cell boards includes a plurality of processors.

9. The computer system of claim 7, wherein the compression/decompression means in at least one of the plurality of cell boards comprises:

means for compressing data transmitted by the memory control means to the communication means; and

means for decompressing data transmitted by the communication means to the memory control means.

10. The computer system of claim 7, wherein the communication means includes the compression/decompression means.

11. A method comprising:

(A) obtaining data from a first memory controller in a multiprocessor computer system;

(B) compressing the data to produce compressed data; and

(C) transmitting the compressed data over a system fabric in the multiprocessor computer system.

12. The method of claim 11, wherein the step (C) is performed by a fabric agent chip in the multiprocessor computer system.

13. The method of claim 11, wherein the step (B) is performed by a fabric agent chip in the multiprocessor computer system.

14. The method of claim 11, further comprising a step of:

(D) decompressing the compressed data to produce the data obtained from the first memory controller.

15. The method of claim 14, further comprising a step of:

(E) providing the data obtained from the first memory controller to a second memory controller in response to a first memory read request issued by the second memory controller.

16. The method of claim 15, further comprising a step of:

(F) providing the data obtained from the first memory controller to a microprocessor in response to a second memory read request issued by the microprocessor.

17. The method of claim 15, further comprising a step of:

(F) storing the data obtained from the first memory controller in a memory controlled by the second memory controller.

18. The method of claim 11, wherein the system fabric comprises a crossbar switch.

19. The method of claim 11, wherein the system fabric comprises a bus.

20. An apparatus comprising:

means for obtaining data from a first memory controller in a multiprocessor computer system;

compression means for compressing the data to produce compressed data; and

transmission means for transmitting the compressed data over a system fabric in the multiprocessor computer system.

21. The apparatus of claim 20, wherein the transmission means comprises a fabric agent chip.

22. The apparatus of claim 20, wherein the compression means comprises a fabric agent chip.

23. The apparatus of claim 20, further comprising:

decompression means for decompressing the compressed data to produce the data obtained from the first memory controller.

24. The apparatus of claim 23, further comprising:

means for providing the data obtained from the first memory controller to a second memory controller in response to a first memory read request issued by the second memory controller.

25. The apparatus of claim 24, further comprising:

means for providing the data obtained from the first memory controller to a microprocessor in response to a second memory read request issued by the microprocessor.

26. The apparatus of claim 24, further comprising:

means for storing the data obtained from the first memory controller in a memory controlled by the second memory controller.